

## REMARKS

Applicant's invention is directed to a method of fabricating a circuit board that includes a non-continuous conductive layer. The method comprises forming a first layer of conductive material over an insulating layer, removing portions of the conductive material of the first layer to define a first circuit pattern and a first rail area that is electrically isolated from the first circuit pattern, and removing portions of the conductive material of the first layer from the first rail area.

In the Office Action, the Examiner objected to the specification, and specifically the Abstract. With this Amendment, applicant has addressed the Examiner's concerns by providing a revised Abstract in accordance with the Examiner's suggestions.

### ***Response to the Double Patenting Rejection***

In the Office Action, the Examiner rejected claims 9-15 under the judicially-created doctrine of obviousness-type double patenting over claims 1-12 of applicant's own prior U.S. Patent No. 6,729,024. Accompanying this paper is a terminal disclaimer signed by an attorney of record. Applicant believes that the terminal disclaimer overcomes this ground of rejection.

### ***Response to the Rejection Under 35 USC §103***

In the Office Action, the Examiner rejected claims 9-10 under 35 USC §103 as unpatentable over "Applicant Admitted Prior Art," ("APA") specifically Figs. 1 and 2 and the Background portion of the specification, or Tsukamoto (US 5841194). The Examiner asserted that "APA" taught a method of fabricating a circuit board "as claimed by the present invention." The Examiner further asserted that Tsukamoto "inherently" disclosed the removal of portions of a conductive material to define a first circuit pattern and a first rail area, and then "removing portions of said conductive material of said first layer from said first rail area," referring to Tsukamoto's Fig. 1.

Applicant submits that neither APA nor Tsukamoto teaches or suggests the presently claimed invention. As shown and discussed by applicant, specification page 6, paragraph [0027], the prior art circuit board depicted in Fig. 2 includes first and second rail areas 201 and 202 that "include a large amount of conductive material" that "stretches from one end of the

substrate to the other." As discussed in the specification, the prior art circuit board depicted in Fig. 2 is susceptible to deformation and warping due to the continuous lengths of conductive material in the rail areas which are thermally cycled during board fabrication. In contrast, as described in the specification at page 7, paragraphs [0028] and [0029], one embodiment of the claimed invention as shown in Fig. 3A includes first and second rail areas 301 and 302 in which all of the conductive material has been removed. In another embodiment shown in Fig. 3B, portions of the conductive material have been removed from the rail areas such that no continuous lengths of conductive materials remain.

The "APA" relied upon by the Examiner does not teach removing portions of conductive material from the first rail area. For purposes of clarification, applicant has amended claim 9 to recite that the removal of portions of the conductive material from the first rail area is such that "no continuous lengths of conductive material remain within said rail area." Nowhere does "APA" teach or suggest such a fabrication method.

Tsukamoto, on the other hand, does not appear to relate to a method of fabricating a circuit board. Rather, Tsukamoto depicts a chip carrier for packaging a semiconductor chip device comprising an insulating board substrate 101 having a peripheral stiffener 106. A semiconductor chip 201 is designed to be inserted into the carrier such that bonding pads on the chip carrier match up with terminal electrodes on the mounted chip. Tsukamoto is so far removed in structure and operation from applicant's invention that it is difficult to follow the Examiner's reasoning.

Assuming that the Examiner is equating one of the bond pads 102 as a "circuit pattern" and another of the bond pads 102 as a "rail area," there is no teaching in Tsukamoto of "removing portions of said conductive material of said first layer to define a first circuit pattern" as recited in claim 9. Tsukamoto is silent concerning how bond pads 102 are formed. Silence in a reference does not form a basis for a conclusion of obviousness. Nor is removal of conductive material "inherent" in Tsukamoto as the Examiner asserts. Bond pads 102 could be formed using a removable mask so that conductive material is deposited only on specific areas. In order for the Examiner to rely upon inherency in a reference, there must be proof that the asserted feature must necessarily and always be formed in the manner asserted. MPEP, §2112. Here, the Examiner has failed to carry that evidentiary burden.

Moreover, Tsukamoto fails to teach or suggest "removing portions of said conductive material ... from said first rail area" as recited in claim 9. Assuming again that the Examiner is asserting that at least one of bond pads 102 corresponds to the recited "first rail area," nothing in Tsukamoto teaches or suggest removing any material whatsoever from bond pads 102. In order to support the Examiner's reasoning, Tsukamoto would have to form a bond pad 102 and then remove at least a portion of the conductive material making up bond pad 102. It is quite clear that Tsukamoto fails to even hint at such a fabrication step. Claims 9 and 10 are patentable over Tsukamoto.

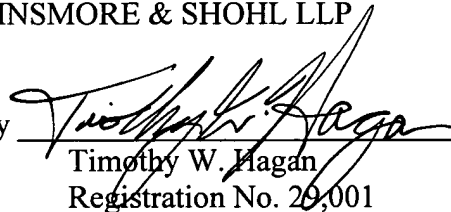
Applicant notes that claims 11-15 have not been rejected on prior art grounds. With the filing of the terminal disclaimer, presumably claims 11-15 are patentable over the cited and applied prior art of record.

For all of the above reasons, applicant submits that claims 9-15 as amended are patentable. Early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

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